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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
ERIC J STRANG	: EXAMINER: SAXENA, AKASH
SERIAL NO: 10/673,507	:
FILED: SEPTEMBER 30, 2003	: GROUP ART UNIT: 2128
FOR: SYSTEM AND METHOD FOR USING FIRST-PRINCIPLES SIMULATION TO CONTROL A SEMICONDUCTOR MANUFACTURING PROCESS	:

APPEAL BRIEF UNDER 37 CFR 41.37

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is an appeal of the final Office Action dated February 7, 2008. A Notice of Appeal was filed on May 19, 2008.

TABLE OF CONTENTS

I. 41.37(C)(1)(I) Real Party of Interest

The real party of interest in this appeal is the assignee Tokyo Electron Limited whose address is Akasaka Biz Tower, 3-1, Akasaka 5-chome, Minato-ku, Tokyo 107-6325, Japan.

II. 41.37(C)(1)(II) Related Appeals and Interferences

There are no related interferences. There are related appeals filed or to be filed in U.S. Serial Nos. 10/673,138; 10/673,467; 10/673,501; 10/673,506; and 10/673,583.

III. 41.37(C)(1)(III) Status of Claims

Claims 1-74 and 78-80 are pending and appealed. Claims 75-77 and 81 are canceled.

Claim 1 stands provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,583 (the '583 application). Claim 1 stands provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,501 (the '501 application). Claim 1 stands provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,138 (the '138 application). Claims 1-81 stand rejected under 35 U.S.C. § 112, first paragraph, as being based on a non-enabling disclosure. Claims 1, 8, and 75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al (U.S. Pat. No. 6,802,045) in view of Jain et al (Mathematical-Physics Engines: Parallel Processing for Modeling and Simulation of Physical Phenomena, 1994, IEEE, pgs. 366-373) and further in view of Tan et al (U.S. Pat. No. 6,263,255). Claims 1-21, 29-30, 32-34, 37-58, 66-67, 69-71, and 74-81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Jain et al. Claims 22 and 59 stand rejected under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Jain et al and Yunemura et al (IEEE Article "Heat Analysis on

Insulated Metal Substrates"). Claims 23-28 and 60-65 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Jain et al and Chen (U.S. Pat. No. 5,719,796). Claims 31, 36, 68, and 73 stand rejected under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Jain et al and Nikoonahad (U.S. Pat. No. 6,812,045). Claims 35 and 72 stand rejected under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Fatke (U.S. Pat. Appl. No. 10/472,436).

IV. 41.37(c)(1)(iv) Status of Amendments

An amendment was filed for this application on October 2, 2007 which resulted in the final Office Action dated February 7, 2008. An amendment after the final rejection was filed on May 19, 2008 canceling Claims 75-77 and 81. A terminal disclaimer was also filed on May 19, 2008. The terminal disclaimer was approved June 11, 2008.

V. 41.37(c)(1)(v) Summary of Claimed Subject Matter

Claim 1, the first of the independent claims appealed, will be treated as a picture claim representing many of the features in the remaining independent claims. Accordingly, a claim chart for support is provided below showing support from the specification for the claim elements.

In short, Claim 1 defines a method of controlling a process performed by a semiconductor processing tool. The method inputs process data ***relating to an actual process being performed*** by the semiconductor processing tool, and inputs a first principles physical model including a set of computer-encoded differential equations. The first principles physical model describes at least one of a basic physical or chemical attribute of the semiconductor processing tool. The method performs first principles simulation ***for the actual process being performed during performance of the actual process*** using the

physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed. The first principles simulation result is ***produced in a time frame shorter in time than the actual process being performed***. The model uses the first principles simulation result obtained during the performance of the actual process to control the actual process performed by the semiconductor processing tool.

Accordingly, Claim 1 makes clear that a first principles simulation result ***for the actual process being performed during performance of the actual process*** is used to control the actual process performed by the semiconductor processing tool. The following is a claim chart comparison of the claim elements to the disclosure in the specification. Emphasis has been added for convenience in some of the longer passages from the specification.

Claim 1	**Support in U.S. Pat. Appl. No. 10/673,507**
A method of controlling a process performed by a semiconductor processing tool, comprising	Specification, numbered paragraph [0011]: According to an aspect of the invention, a method of controlling a process performed by a semiconductor processing tool includes inputting data relating to a process performed by the semiconductor processing tool, and inputting a first principles physical model relating to the semiconductor processing tool. First principles simulation is then performed using the input data and the physical model to provide a first principles simulation result, and the first principles simulation result is used to control the process performed by the semiconductor processing tool.

inputting process data relating to an actual process being performed by the semiconductor processing tool	Specification, numbered paragraph [0032]: Data input device 104 is a device for collecting data relating to a process performed by the semiconductor processing tool 102 ***and inputting the collected data to the first principles simulation processor 106.*** . . . In one embodiment, the data input device 104 may be implemented as a physical sensor for collecting data about the semiconductor processing tool 102 itself, and/or the environment contained within a chamber of the tool. Such data may include fluid mechanic data such as gas velocities and pressures at various locations within the process chamber, electrical data such as voltage, current, and impedance at various locations within the electrical system of the process chamber, chemical data such as specie concentrations and reaction chemistries at various locations within the process chamber, thermal data such as gas temperature, surface temperature, and surface heat flux at various locations within the process chamber, plasma processing data (when plasma is utilized) such as a plasma density (obtained, for example, from a Langmuir probe), an ion energy (obtained, for example, from an ion energy spectrum analyzer), and mechanical data such as pressure, deflection, stress, and strain at various locations within the process chamber. Specification, numbered paragraph [0039]: FIG. 2 is a flow chart showing a process for using first principles simulation techniques to-facilitate a process performed by a semiconductor processing tool in accordance with an embodiment of the present invention. The process shown in FIG. 2 may be run on the first principles simulation processor 104 of FIG. 1, for example. As seen in FIG. 2, the process begins in step 201 with the inputting of data related to a process performed by the semiconductor processing tool 102. As discussed above, the input data may be data relating to physical attributes of the tool/tool environment and/or data relating to a process performed by the tool on a semiconductor wafer or results of such process. As also described above, ***the input data may be directly input from a physical sensor or metrology tool coupled to the first principles simulation processor 104***, or indirectly input from a manual input device or database.

inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;	Specification, numbered paragraph [0035]: First principles physical model 106 is a model of the physical attributes of the tool and tool environment as well ***as the fundamental equations necessary to perform first principles simulation*** and provide a simulation result for facilitating a process performed by the semiconductor processing tool. Thus, the first principles physical model 106 depends to some extent on the type of semiconductor processing tool 102 analyzed as well as the process performed in the tool. For example, the physical model 106 may include a spatially resolved model of the physical geometry of the tool 102, which is different, for example, for a chemical vapor deposition (CVD) chamber and a diffusion furnace. Similarly, the first principles equations necessary to compute flow fields are quite different than those necessary to compute temperature fields. The physical model 106 may be a model as implemented in commercially available software, such as ANSYS, of ANSYS Inc., Southpointe, 275 Technology Drive Canonsburg, Pa. 15317, FLUENT, of Fluent Inc., 10 Cavendish Conn. Centerra Park, Lebanon, N.H. 03766, or CFD-ACE+, of CFD Research Corp., 215 Wynn Dr., Huntsville, Ala. 35805, to compute flow fields, electromagnetic fields, temperature fields, chemistry, surface chemistry (i.e. etch surface chemistry or deposition surface chemistry). However, special purpose or custom models developed from first principles to resolve these and other details within the processing system may also be used. Specification, numbered paragraph [0036]: First principles simulations in the present invention include, but are not limited to, simulations of electro-magnetic fields derived from ***Maxwell's equations, continuum simulations, for example, for mass, momentum, and energy transport derived from continuity, the Navier-Stokes equation*** and the First Law of Thermodynamics, as well as atomistic simulations derived from the Boltzmann equation, such as for example Monte Carlo simulations of rarefied gases (see Bird, G. A. 1994. Molecular gas dynamics and the direct simulation of gas flows, Clarendon Press).

performing first principles simulation for the actual process being performed during performance of the actual process using the physical model	Specification, numbered paragraph [0012]: A first principles simulation processor is configured to input a first principles physical model relating to the semiconductor processing tool, and perform first principles simulation using the input data and the physical model to provide a first principles simulation result. The first principles simulation result is used to control the process performed by the semiconductor processing tool. Specification, numbered paragraph [0036]: First principles simulation processor 108 is a processing device that applies data input from the data input device 104 to the first principles physical model 108 to execute a first principles simulation. Specifically, the first principles simulation processor 108 may use the data provided by the data input device 104 to set initial conditions and/or boundary conditions for the first principles physical model 106, which is then executed by the simulation module. Specification, numbered paragraph [0057]: In this embodiment, steady-state simulations are repeatedly run concurrently with the process by using the physical sensor measurements to repeatedly update boundary conditions of the first principles simulation model.
to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed,	Specification, numbered paragraph [0036]: The output of the first principles simulation processor 108 is a simulation result that is used to facilitate a process performed by the semiconductor processing tool 102. For example, the simulation result may be used to facilitate process development, process control and fault detection as well as to provide virtual sensor outputs that facilitate tool processes, as will be further described below.

said first principles simulation result being produced in a time frame shorter in time than the actual process being performed; and	Specification, numbered paragraph [0041]: In step 205, the first principles simulation processor 108 uses the input data of step 201 and the first principles physical model of step 203 to execute a first principles simulation and provide a simulation result. Step 205 may be performed either concurrently with or not concurrently with the process performed by the semiconductor processing tool. For example, simulations that can be performed at short solution times may be run concurrently with a tool process, and results used to control the process. More computationally intensive simulations may be performed not concurrently with the tool process and the simulation result may be stored in a library for later retrieval. In one embodiment, step 205 includes using the input data of step 201 to set initial and/or boundary conditions for the physical model provided in step 205. Specification, numbered paragraph [0057]: In this embodiment, steady-state simulations are repeatedly run concurrently with the process by using the physical sensor measurements to repeatedly update boundary conditions of the first principles simulation model.

using the first principles simulation result obtained during the performance of the actual process to control the actual process performed by the semiconductor processing tool.	Specification, numbered paragraph [0012]: The first principles simulation result is used to control the process performed by the semiconductor processing tool. Specification, numbered paragraph [0042]: Once the simulation is executed, the simulation result is used to facilitate a process performed by the semiconductor processing tool 102. As used herein, the term "facilitate a process performed by the semiconductor processing tool" includes using the simulation result for example to detect a fault in the process, to control the process, to characterize the process for manufacturing runs, to provide virtual sensor readings relating to the process, or any other use of the simulation result in conjunction with facilitating a process performed by the semiconductor processing tool 102. Specification, numbered paragraph [0048]: The present inventors have also discovered that the network architecture of FIG. 3 provides the ability to distribute model results done at one processing tool 102 for one condition set, to other similar or identical tools operating later under the same or similar conditions, so redundant simulations are eliminated. Running simulations only for unique processing conditions at on-tool and standalone modules and re-using results from similar tools that have already known simulated solutions allows for rapid development of lookup libraries containing results that can be used for diagnostics and control over a large range of processing conditions. Further, the reuse of the known solutions as initial conditions for first principles simulation reduces the computational requirements and facilitates the production of simulated solutions in a time frame consistent with on-line control. Similarly, the network architecture of FIG. 3 also provides the ability to propagate changes and refinements made to physical models and model input parameters from one simulation module to others in the network. ***For example, if during process runs and parallel executions of a model it is determined that some input parameters need to be changed, then these changes can be propagated to all other simulation modules and tools via the network.***

Claim 38 defines a system which is similar to the method of Claim 1. Thus, the features of Claim 38 are supported in the specification by numbered paragraphs [0011],

[0012], [0032]. [0035], [0036], [0039], [0041], [0042], [0048], and [0057].

Claim 78 defines at least one of non-volatile media and volatile media containing program instructions for execution on a processor, which is similar to method Claim 1. Thus, the features of Claim 78 are supported in the specification by numbered paragraphs [0011], [0012], [0032]. [0035], [0036], [0039], [0041], [0042], [0048], and [0057].

VI. 41.37(C)(1)(VI) Grounds of Rejection for Review

Whether the rejection of Claim 1 under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,583 (the '583 application) should be reversed. Whether the rejection of Claim under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,501 (the '501 application) should be reversed. Whether the rejection of Claim 1 under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,138 (the '138 application) should be reversed. Whether the rejection of Claims 1-81 under 35 U.S.C. § 112, first paragraph, as being based on a non-enabling disclosure should be reversed. Whether the rejection of Claims 1, 8, and 75 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Jain et al and further in view of Tan et al should be reversed. Whether the rejection of Claims 1-21, 29-30, 32-34, 37-58, 66-67, 69-71, and 74-81 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Jain et al should be reversed. Whether the rejection of Claims 22 and 59 under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Jain et al and Yunemura et al should be reversed. Whether the rejection of Claims 23-28 and 60-65 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Jain et al and Chen should be reversed.

Whether the rejection of Claims 31, 36, 68, and 73 under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Jain et al and Nikoonahad should be reversed.

Whether the rejection of Claims 35 and 72 under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Fatke should be reversed.

VII. 41.37(C)(1)(VII) ARGUMENTS

A. Regarding the 35 USC 112 1st Paragraph Rejection of Claims 1-74 and 78-80

Briefly recapitulating, Claim 1 defines a method of controlling a process performed by a semiconductor processing tool, including:

> 1) inputting process data relating to an actual process being performed by the semiconductor processing tool,
>
> 2) inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool,
>
> 3) performing first principles simulation for the actual process being performed ***during performance of the actual process*** using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, ***said first principles simulation result being produced in a time frame shorter in time than the actual process being performed,*** and
>
> 4) using the first principles simulation result ***obtained during the performance of the actual process*** to control the actual process being performed by the semiconductor processing tool.

The claim defines clearly a process where data input from an actual process being performed is used for producing a first principles simulation result, produced for the actual process being performed during performance of the actual process. The result obtained is produced in a time frame shorter in time than the actual process being performed. The result obtained is then used to control the actual process being performed by the semiconductor processing tool.

M.P.E.P. 2164.01 states that the test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art ***without undue experimentation***. Appellant submits that details of 1) inputting the process data and 2) inputting the first principles physical model including what basic physical and chemical attribute of the semiconductor processing tool are used are disclosed in Appellant's filed specification. For instance, details of inputting data are given for example at numbered paragraphs [0032] and [0033], which state:

> Data input device 104 is a device for collecting data relating to a process performed by the semiconductor processing tool 102 and inputting the collected data to the first principles simulation processor 106. The process performed by the semiconductor process tool 102 may be a characterization process (i.e. process design or development), a cleaning process, a production process, or any other process performed by the semiconductor processing tool. In one embodiment, the data input device 104 may be implemented as a physical sensor for collecting data about the semiconductor processing tool 102 itself, and/or the environment contained within a chamber of the tool. Such data may include fluid mechanic data such as gas velocities and pressures at various locations within the process chamber, electrical data such as voltage, current, and impedance at various locations within the electrical system of the process chamber, chemical data such as specie concentrations and reaction chemistries at various locations within the process chamber, thermal data such as gas temperature, surface temperature, and surface heat flux at various locations within the process chamber, plasma processing data (when plasma is utilized) such as a plasma density (obtained, for example, from a Langmuir probe), an ion energy (obtained, for example, from an ion energy spectrum analyzer), and mechanical data such as pressure, deflection, stress, and strain at various locations within the process chamber.
>
> In addition to the tool and tool environment data, the data input device 104 may collect data relating to the process itself, or process results obtained on a semiconductor wafer that the tool 102 is performing a process on. In one embodiment, data input device 104 is implemented as a metrology tool coupled to the semiconductor processing tool 102. The metrology tool may be configured to measure process performance parameters such as: etch rate, deposition rate, etch selectivity (ratio of the rate at which a first material is etched to the rate at which a second material is etched), an etch critical dimension (e.g. length or width of feature), an etch feature anisotropy (e.g. etch feature sidewall profile), a film property (e.g. film stress, porosity, etc.), a mask (e.g. photoresist) film thickness, a mask (e.g. photoresist) pattern critical dimension, or any other parameter of a process performed by the semiconductor processing tool 102.

Details of inputting a first principles physical model for performing the first principles simulation result are given for example at numbered paragraphs [0035] and [0036] which state that:

> First principles physical model 106 is a model of the physical attributes of the tool and tool environment as well as the fundamental equations necessary to perform first principles simulation and provide a simulation result for facilitating a process performed by the semiconductor processing tool. Thus, the first principles physical model 106 depends to some extent on the type of semiconductor processing tool 102 analyzed as well as the process performed in the tool. For example, the physical model 106 may include a spatially resolved model of the physical geometry of the tool 102, which is different, for example, for a chemical vapor deposition (CVD) chamber and a diffusion furnace. Similarly, the first principles equations necessary to compute flow fields are quite different than those necessary to compute temperature fields. The physical model 106 may be a model as implemented in commercially available software, such as ANSYS, of ANSYS Inc., Southpointe, 275 Technology Drive Canonsburg, PA 15317, FLUENT, of Fluent Inc., 10 Cavendish Ct. Centerra Park, Lebanon, NH 03766, or CFD-ACE+, of CFD Research Corp., 215 Wynn Dr., Huntsville, AL 35805, to compute flow fields, electro-magnetic fields, temperature fields, chemistry, surface chemistry (i.e. etch surface chemistry or deposition surface chemistry). However, special purpose or custom models developed from first principles to resolve these and other details within the processing system may also be used.
>
> First principles simulation processor 108 is a processing device that applies data input from the data input device 104 to the first principles physical model 108 to execute a first principles simulation. Specifically, the first principles simulation processor 108 may use the data provided by the data input device 104 to set initial conditions and/or boundary conditions for the first principles physical model 106, which is then executed by the simulation module. First principles simulations in the present invention include, but are not limited to, simulations of electro-magnetic fields derived from Maxwell's equations, continuum simulations, for example, for mass, momentum, and energy transport derived from continuity, the Navier-Stokes equation and the First Law of Thermodynamics, as well as atomistic simulations derived from the Boltzmann equation, such as for example Monte Carlo simulations of rarefied gases (see Bird, G.A. 1994. Molecular gas dynamics and the direct simulation of gas flows, Clarendon Press). First principles simulation processor 108 may be implemented as a processor or workstation physically integrated with the semiconductor processing tool 102, or as a general purpose computer system such as the computer system 1401 of Figure 14. The output of the first principles simulation processor 108 is a simulation result that is used to facilitate a process performed by the semiconductor processing tool 102. For example, the simulation result may be used to facilitate process

development, process control and fault detection as well as to provide virtual sensor outputs that facilitate tool processes, as will be further described below.

Thus, one of ordinary skill in the art, from the detailed information provided in the specification as to the data input and as to the commercially availability of software programs, would **not** have to use undue experimentation to apply the respective physical attributes that each model is tailored to accept in order to perform the claimed inputting a first principles physical model step.

The examiner requested details of the models which lead to the unexpected result of being able to avoid the lengthy time conventionally required for the generation of a first principles model simulation. See page 10 of the Office Action. Appellant points out that the subject matter of Claims 15-19 and 79 as procedures by which the unexpected results of the invention are achieved. It is not the details of the models, but rather the details as to how the model calculations are implemented which reduce the time for calculations. For instance, the disclosed characteristics in the specification which permit simulation results to be obtained in a time frame compatible with using the first principles model simulation result for real time process control are enumerated below with reference to the numbered paragraphs in the filed specification:

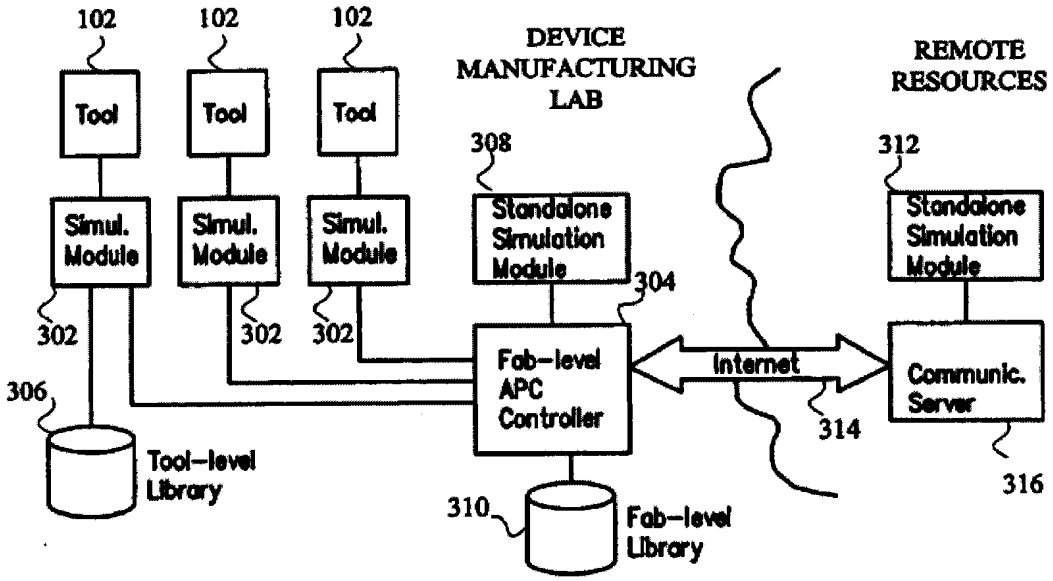
1) the use of interconnected resources inside a semiconductor device manufacturing facility to perform the first principles simulation (see specification, numbered paragraph [0043] and Figure 3, both reproduced below),

2) the use of code parallelization among interconnected computational resources inside the semiconductor device manufacturing facility (see specification, numbered paragraphs [0047] and [0048] reproduced below),

3) the sharing of simulation information among interconnected resources inside the semiconductor device manufacturing facility (see specification, numbered paragraphs [0047] and [0048] reproduced below), and

4) the reduction in redundant execution of substantially similar first principles simulations by different resources the reuse of known solutions as initial conditions for the first principles simulation, as features which used singularly or in combination lead to a simulation result in a time frame consistent with real time process control in a semiconductor processing tool (see specification, numbered paragraphs [0047] and [0048] reproduced below).

Figure 3



[0043] FIG. 3 is a block diagram of a network architecture that may be used to provide first principles simulation techniques to facilitate a process performed by a semiconductor processing tool in accordance with an embodiment of the present invention. As seen in this figure, the network architecture includes a device manufacturing fab connected to remote resources via the Internet 314. The device manufacturing fab includes a plurality of semiconductor processing tools 102 connected to respective simulation modules 302. As described with respect to FIG. 1, each semiconductor processing tool 102 is a tool for performing a process related to manufacturing a semiconductor device such as an integrated circuit. Each simulation module 302 is a computer, workstation, or other processing device capable of executing first principles simulation techniques to facilitate a process performed by a semiconductor processing tool 102. Thus, each simulation module 302 includes the first principles physical model 106 and the first principles simulation processor 108 described with respect to FIG. 1, as well as any other hardware and/or software that may be helpful for executing first principles simulations. Moreover, simulation modules 302 are configured to communicate with the fab-level advanced process control (APC) controller

using any known network communication protocol. Each simulation module 302 may be implemented as a general purpose computer such as the computer system 1401 of FIG. 14.

[0047] The present inventors have discovered that the network configuration of FIG. 3 provides computational and storage resource sharing that allows a broad range of first principles simulation results at reasonable solution speeds, thus providing meaningful on-tool simulation capabilities that can facilitate processes performed by the tool. Specifically, while simple simulations may be executed by a tool's dedicated simulation module, complex simulations requiring greater computational resources may be executed using code parallelization techniques on multiple simulation modules in the network that may be on-tool or standalone. Even on-tool simulation modules in equipment currently under preventive maintenance may be used as a shared computational resource, provided there is power to the simulation module. Similarly, simulation results used for later lookup can be stored in libraries (e.g. storage devices) anywhere in the fab network, and accessed by all tools when lookups of diagnostic or control data are made.

[0048] The present inventors have also discovered that the network architecture of FIG. 3 provides the ability to distribute model results done at one processing tool 102 for one condition set, to other similar or identical tools operating later under the same or similar conditions, so redundant simulations are eliminated. Running simulations only for unique processing conditions at on-tool and standalone modules and re-using results from similar tools that have already known simulated solutions allows for rapid development of lookup libraries containing results that can be used for diagnostics and control over a large range of processing conditions. Further, the reuse of the known solutions as initial conditions for first principles simulation reduces the computational requirements and facilitates the production of simulated solutions in a time frame consistent with on-line control. Similarly, the network architecture of FIG. 3 also provides the ability to propagate changes and refinements made to physical models and model input parameters from one simulation module to others in the network. For example, if during process runs and parallel executions of a model it is determined that some input parameters need to be changed, then these changes can be propagated to all other simulation modules and tools via the network.

Hence, it is respectfully submitted that, in view of the disclosure of commercial software available for the different physical models disclosed in the specification and in view of the disclosure of procedures by which the time for producing a first principles model simulation result can be reduced, the invention does not require undue experimentation.

Accordingly, the 35 U.S.C. 112, first paragraph, rejection of Claims 1-74 and 78-80 should be reversed.

B. Regarding the 35 USC 103 Rejection of Claim 1, 8, and 75 over Sonderman et al, Jain et al, and Tan et al

The Office Action makes clear on pages 3 and 4 that the Examiner and the Appellant disagree as to whether the subscripts in Sonderman et al S_i associated with the silicon wafer disclosure refers to process control for the same wafer being processed or process control for subsequent wafers. The Examiner's position is that Sonderman et al would have used S_{i+1} to designate subsequent wafers.

Yet, Appellant respectfully points out that, at col. 9, lines 46-51, Sonderman et al specifically states:

> The system 100 ***then*** optimizes the simulation (described above) to find more optimal process target (T_i) for each silicon wafer, ***S_i to be processed***. These target values are then used *t*o generate ***new control inputs, X_{Ti},*** on the line 805 to control ***a subsequent process of a silicon wafer S_i***. [Emphasis added]

The plain reading of this section of Sonderman et al is that the system 100 ***then*** (e.g., at time T1) optimizes the simulation for each silicon wafer, ***S_i to be processed*** (e.g., later at time T2). In other words, the simulation results of Sonderman et al produce a new control input for each silicon wafer ***to be processed***. Thus, Appellant respectfully submits that Sonderman et al teach performing a simulation result for a process to be performed ***before*** performance of the actual process, and do **not** teach the claimed performing first principles simulation ***for the actual process being performed during performance of the actual process***.[1]

Other sections of Sonderman et al support Appellant's position on this matter that the simulation results in Sonderman et al are made prior to controlling a subsequent process. For

[1] Appellant also point out that Sonderman et al do not disclose or suggest a first principles simulation.

instance, Figure 4 of Sonderman et al (reproduced below) shows that the simulation results are produced ***ahead of performing a process*** and thus have to be based on historical data.

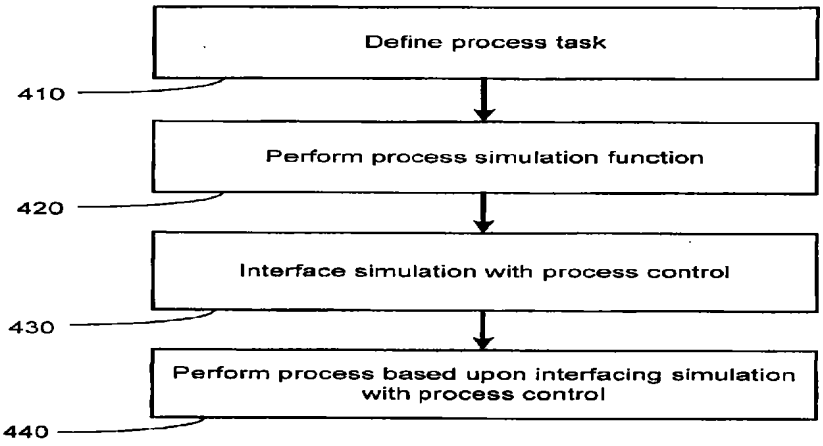


FIGURE 4

With reference to Figure 4, Sonderman et al disclose at col. 6, lines 24-47:

> Turning now to FIG. 4, a flow chart representation of the methods in accordance with the present invention is illustrated. In one embodiment, ***the system 100 defines a process task that is to be performed (block 410).*** The process task may be a photolithography process, an etching process, and the like. ***The system 100 then performs a process simulation function*** (block 420). A more detailed description of the process simulation function described in block 420, is illustrated below. In one embodiment, a simulation data set results from the execution of the process simulation function.
>
> ***Once the system 100 performs the process simulation function, the system 100 performs an interfacing function***, which facilitates interfacing of the simulation data with the process control environment 180 (block 430). The process control environment 180 can utilize the simulation data in order to modify or define manufacturing control parameters that control the actual processing steps performed by the system 100. ***Once the system 100 interfaces the simulation data with the process control environment 180, the system 100 then performs a manufacturing process*** based upon the manufacturing parameters defined by the process control environment 180 (block 440). [Emphasis added]

Hence, the process flow in Sonderman et al is straightforward:

1) define a process to be modeled,

2) model the simulation result,

3) interface simulation result to processor, and then

4) run the process under control based on the pre-existing simulation result.

In the final Office Action, the examiner disagreed with this interpretation of Sonderman et al. On page 6 of the Office Action, the examiner pointed out a part of Sonderman et al's disclosure with emphasis added by underscoring which was believed by the examiner to support his position on this matter. This characterization is repeated below for the sake of convenience with the examiner's emphasis.

> Furthermore, the simulation environment 210 can be used for feedback modification of control parameters invoked by the process control environment 180. For example, the manufacturing environment 170 can send metrology data results into the simulation environment 210. The simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment 180. A feedback loop in then completed when the process control environment 180 sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers. {Examiner's emphasis added.}

Appellant respectfully points out that this description in Sonderman et al is a description of a **feedback loop** as Sonderman et al describe just below that portion which the examiner emphasized. Feedback modification is by definition the control of future wafers based on what has already occurred to a previous wafer. Hence, this section supports rather than refutes Appellant's position on this matter.

Accordingly, Appellant respectfully submits that Sonderman et al do not disclose and indeed ***teach away*** from the present invention where data input from an actual process being performed is used for producing a first principles simulation result, which is produced for the actual process being performed during performance of the actual process for control of the actual process.

The deficiencies in Sonderman et al are not overcome by Jain et al. The Office Action in rejecting the present claims supplements the teachings of Sonderman et al with the teachings of Jain et al for their teaching of computer encoded differential equations in a mathematical physical engine (MPE) which can be applied to wafer processing. See Office Action, page 16. Jain et al describe at pages 372-373 that:

> We ***propose*** a wafer scale implementation of the MPE. The starting point would be a dedicated processing cell, optimized specifically for the PDE arithmetic and data routing. Because of the relative simplicity of the cell, it is expected that extremely large arrays (8x8 to 32x32) ***could be*** successfully processed on a single piece of silicon using Wafer Scale Integration techniques. In fact, we have already laid the foundation for the development of such a processing cell. Our Universal Multiply-Subtract-Add [11] ***could be*** adapted for this first cell design. Similarly, our nonlinear coprocessor cell [12]-[14] ***might be used*** in conjunction with the UMSA to provide advanced mathematical functions. As suggested in Fig. 2, there would be ***courtyards of processors***, each with two interconnection networks and two memory banks. 2-D, 3-D, and 4-D problems could then be mapped for parallel computations. Since inter-processor delays are very small (say a few ns), extremely high speeds could be achieved. This, together with the high degree of parallelism, would result also in high throughout. We ***envision*** 100 to 1000 processors (on one wafer) forming a wafer scale MPE. At a clock frequency of 50 MHz, a single wafer could achieve up to 20 GFLOPs performance. With our nonlinear coprocessor added, each instruction could equate to multiple floating point operations.
>
> Furthermore, because of the extendible architecture, several wafers ***could be*** interconnected as shown in Fig. 5 to construct a "stacked" MPE wafer system (SMPE). Note that no vertical interconnects within the stack of wafers are expected. Tens to hundreds of GFLOPs performance in a volume the size of a desk-top computer [15] ***could*** thus be achieved. However, ***these predictions*** ignore the likely technical advances in the next five years; a tenfold further increase in performance ***might be achievable***. [Emphasis Added]

Thus, as emphasized above, the proposed development work in Jain requires the development of ***futuristic*** computational equipment which one of ordinary skill in the art would be reluctant to implement or utilize for the rigorous standards needed in semiconductor manufacturing.

Appellant's position in this matter is corroborated by Tan et al. Tan et al also teach the use on an existing process model for feedback or feed forward processing. In feedback control, by definition, the results of a process step are provided to subsequent wafer. In feed forward control, the results of a prior process step are used to adjust a subsequent process being run of the wafer. Tan et al describe:

> The illustrative APC Framework 200 includes a process model 202 that receives ***feed-forward and feed-back data*** and calculates a processing parameter. The illustrative portion of the APC Framework 200 includes two measurement devices, in particular a pre-process metrology machine 204 and a post-processing metrology machine 206. The pre-process metrology machine 204 performs a measurement on a material prior to processing in a processing machine 208 and sends the measurement, as feed-forward data, to the process model 202. The processing machine 208 sends processed material to the post-processing metrology machine 206 ***to measure post-process data which is sent to the process model 202 as feedback data.***
>
> Referring to FIG. 4, a schematic block diagram shows material flow of a processing step 400 of a semiconductor manufacturing process from a process engineer perspective. An APC plan 402 retrieves a process model from the data store 306, then executes a parameter calculation algorithm 404. The APC plan 402 gives the calculated parameters to a machine 406 and directs the machine 406 to execute the process. The machine 406 issues a signal to the APC plan 402 ***when the process execution is complete.*** The APC plan 402 sends the calculated parameters to the data history store 310 of the historical database 312.
>
> Referring to FIG. 5, a schematic block diagram shows material flow of a post-process measurement step 500 of a semiconductor manufacturing process from a process engineer perspective. An APC plan 502 sends a message to a machine 504 instructing the machine 504 to measure a post-processed material. The machine 504 sends measurement data to the APC plan 502. The APC plan 502 retrieves an old process model from the data store 306. The APC plan 502 executes a model update algorithm 506. The APC plan 502 ***stores an updated model in the data store 306 for usage in the processing step 400.*** The APC plan 502 sends new model data to the data history store 310 of the historical database 312. [Emphasis added.]

Thus, Tan et al use post-process data to update a model for a subsequent process step. Hence, Tan et al do not overcome the deficiencies of Sonderman et al. Accordingly, even if Tan et al were combined with the other art of record, the combination would not disclose or

suggest that a simulation result is produced in a time frame shorter in time than the actual process being performed, as claimed.

Appellant's position on these matters is also supported by Kee et al. In the outstanding Office Action, the examiner indicated that he found no connection or legal basis for considering the teachings of Kee et al. Recently published guidelines for the Patent and Trademark Office, published in Federal Register Vol. 72, No. 195, on Wednesday October 10, 2007entitled: "Examination Guidelines for Determining Obviousness under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International v. Teleflex Inc," indicate that:

> Office personnel should consider all rebuttal evidence that is timely presented by the Applicants when reevaluating any obviousness determination. Rebuttal evidence may include evidence of "secondary considerations," such as "commercial success, long felt but unsolved needs, [and] failure of others", and may also include evidence of unexpected results. Office personnel must articulate findings of fact that support the rationale relied upon in an obviousness rejection. As a result, Applicants are likely to submit evidence to rebut the fact finding made by Office personnel. For example, in the case of a claim to a combination, Applicants may submit evidence or argument to demonstrate that:
>
> (1) one of ordinary skill in the art could not have combined the claimed elements by known methods (e.g., ***due to technological difficulties***);
>
> (2) the elements in combination do not merely perform the function that each element performs separately; or
>
> (3) the results of the claimed combination were ***unexpected***.
>
> Once the Applicant has presented rebuttal evidence, Office personnel should reconsider any initial obviousness determination in view of the entire record. All the rejections of record and proposed rejections and their bases should be reviewed to confirm the continued viability. The Office action should clearly communicate the Office's findings and conclusions, articulating how the conclusions are supported by the findings. [Emphasis Added.]

M.P.E.P. § 2143.01(II) indicates that all teachings in the prior art must be considered. M.P.E.P. 2141.03 indicates that the examiner must ascertain what would have been obvious to one of ordinary skill in the art at the time of the invention. Hence, for all these legal

considerations, Kee et al is presented as rebuttal evidence for the non-obviousness of the claims.

Specifically, the prior art Kee et al reference is evidence of the **technological difficulties** involved in producing a first principles model simulation result and, under the published guidelines, should be considered. The prior art Kee et al reference represents what one of ordinary skill in the art would have known and would have expected at the time of the invention and, under the M.P.E.P., should be considered.

Kee et al deal with the process control of a Rapid Thermal Processing (RTP) tool and do **not** use real time modeling. RTP tools are tools used in semiconductor manufacturing. Kee et al in detail disclose that:

> The modeling apparatus 101 of the instant invention may also be used to perform an inverse analysis to establish the boundary conditions or parameter values required to achieve a certain function of the thermal system. This allows the apparatus to be used to establish the appropriate process parameters and boundary conditions for the thermal system modeled. In accordance with the instant invention, the inverse analysis can be directly carried out by the modeling apparatus ***rather than using the conventional approach, which merely solves the direct problem repeatedly, in a lengthy and costly iterative process***, to determine appropriate input parameters to achieve a desired result. In other words, in accordance with the instant invention, ***once a particular thermal process is modeled for a particular set of control parameters***, the device may then be used to automatically obtain the necessary control parameters to achieve a desired result by providing the modeling apparatus with parameters corresponding to the desired result.
>
> To carry out the inverse analysis, the modeling apparatus 101 includes an inverse parameter input section 104 also connected to input device 103. A user inputs into the modeling apparatus 101 parameters corresponding to desired results, e.g., desired temperature characteristics of the system, which are stored in memory 108. The processing unit 110, under control of modeling program 111, ***uses the previously generated model*** of the thermal system and the parameters held in memory 108 and derives or predicts particular control parameters to meet the constraints entered through the inverse parameter input section 104. This process is more fully described below in connection with the examples provided.[2] [Emphasis added.]

[2] Kee et al, col. 4, lines 21-50.

Hence, Kee et al explicitly disclose that a ***previously generated*** model of the thermal system is used to design and control the thermal system. Kee et al exemplify the difficulties of a "conventional approach" which solves spectral radiation transport equations through "a lengthy and costly iterative process." These problems forced Kee et al to use ***pre-generated model results*** for a control process of a RTP process.

The examiner in the final Office Action did not apply but rather noted the IEEE 1990 paper by Su-shing Chen, "AEMPES: An expert system for in-situ diagnostics and process monitoring," hereinafter referred to as AEMPS, as evidence that the newly added limitation (said first principles simulation result being produced in a time frame shorter in time than the actual process being performed) is known in the art. Yet, AEMPS describes the use of simulation in neural network environment used to "learn processes and the equipment model." See page 120, section 4. AEMPS describes in section 4 that "a rule-based expert system provides human interfaces and high-level decision support." Accordingly, AEMPS does **not** describe a first principles simulation result, but rather describes a neural network learning-based simulation. Accordingly, a system such as in AEMPS which learns a behavior and establishes rules based on the behavior would be used in a feedback control (see section 4 of AEMPS). Such a system would **not** 1) produce a first principles simulation result or 2) produce a first principles simulation result during the performance of the actual process to control the actual process performed by the semiconductor processing tool.

Moreover, AEMPS describes in section 2 (regarding manufacturing automation) that it is **not known** how to couple computer aided design, the integration of a manufacturing line, and its simulator together, and that it is **not known** how "to complete integration of manufacturing lines with their simulators." Hence, like Jain et al, AEMPS describes a ***futuristic*** system under development. Even if for the sake of argument it were supposed that

the AEMPS system was a first principles simulation result (which it is not), one of ordinary skill in the art would be reluctant to implement or utilize the AEMPS system for the rigorous standards needed in semiconductor manufacturing.

The examiner in the final Office Action also noted appellant's disclosure at numbered paragraphs [0004] and [005] in the specification as an apparent admission that the feature of a first principles simulation result being produced in a time frame shorter in time than the actual process being performed was a feature known in the art. Yet, the specification describes this material as being background material and makes no indication that what the present inventors recognized and described in the background section was known to others or would in any other way qualify as 35 U.S.C. § 102 prior art.

More importantly, numbered paragraphs [0004] and [005] indicate at most that the times for a large number of simulations ***typically done in the tool design stage*** are comparable to wafer or wafer cassette processing times. There is no statement here regarding how long the times would be for a process control simulation. Further, numbered paragraphs [0004] and [005] indicate that, at the time of the invention, there were serious impediments which would mean that it would not be possible, prior to the invention, to produce a first principles simulation result in a time frame shorter in time than the actual process being performed.

> **[0004]** These industry and manufacturing challenges have led to interest in more use of computer based modeling and simulation in the semiconductor manufacturing industry. Computer-based modeling and simulation are increasingly being used for prediction of tool performance during the semiconductor manufacturing tool design process. The use of modeling allows the reduction of both cost and time involved in the tool development cycle. Modeling in many disciplines, such as stress, thermal, magnetics, etc., has reached a level of maturity where it can be trusted to provide accurate answers to design questions. Moreover, computer power has been increasing rapidly along with the development of new solution algorithms, both of which resulted in reduction of time required to obtain a simulation result. ***Indeed, the present inventors have recognized that a large number of simulations***

> ***typically done in the tool design stage can presently be run in times comparable to wafer or wafer cassette processing times.*** These trends have led to the suggestion that simulation capability typically used only for tool design can be implemented directly on the tool itself to aid in various processes performed by the tool. For example, the 2001 International Technology Roadmap for Semiconductors ***identifies issues impeding the development of on-tool integrated simulation capability*** as an enabling technology for manufacturing very small features in future semiconductor devices.
>
> **[0005]** Indeed, ***the failure of industry to implement on-tool simulation to facilitate tool processes is primarily due to the need for computational resources capable of performing the simulations in a reasonable time.*** Specifically, the processor capabilities currently dedicated to semiconductor manufacturing tools are typically limited to diagnostic and control functions, and therefore could only perform relatively simple simulations. Thus, the semiconductor manufacturing industry has perceived ***a need to provide powerful dedicated computers in order to realize meaningful on-tool simulation capabilities.*** However, dedication of such a computer to the semiconductor processing tool results in wasted computational resources when the tool runs processes that use simple simulations, or no simulations at all. This inefficient use of an expensive computational resource has been ***a major impediment to implementation of simulation capabilities on semiconductor processing tools.*** [Emphasis added.]

Hence, Tan et al, Jain et al, Kee et al, AEMPES, and the background section of the specification **all** discredit any suggestion that the examiner may have read from the disclosure of Sonderman et al for real-time simulation and control of an actual process being performed.

The Supreme Court in *KSR International Co. v. Teleflex Inc. et al. 2007 U.S. LEXIS 4745* reinforced the role of *Graham* factors, teaching away and elements working together in an unexpected and fruitful manner in deciding obviousness. The Court stated that:

> In *United States v. Adams*, 383 U. S. 39, 40 (1966), a companion case to *Graham*, the Court considered the obviousness of a wet battery that varied from prior designs in two ways: It contained water, rather than the acids conventionally employed in storage batteries; and its electrodes were magnesium and cuprous chloride, rather than zinc and silver chloride. The Court recognized that when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result. 383 U. S., at 50-51. It nevertheless rejected the Government's claim that Adams's battery was obvious. The Court relied upon the corollary principle that when the prior art ***teaches away*** from combining certain known

> elements, discovery of a successful means of combining them is more likely to be nonobvious. *Id.*, at 51-52. When Adams designed his battery, the prior art warned that risks were involved in using the types of electrodes he employed. The fact that the elements worked together in ***an unexpected and fruitful manner*** supported the conclusion that Adams's design was ***not obvious*** to those skilled in the art. [Emphasis added.]

In the present situation, the claimed elements worked together in ***an unexpected and fruitful manner*** as compared to the prior art. For example, since in Sonderman et al there are ***new control inputs*** for each subsequent wafer, one can not compensate for real time excursions from the existing model occurring while the wafer is being processed. In other words, the historically lengthy time for generation of a first principles model simulation would mean that, in Sonderman et al, one is prevented from realizing a real time process control based on a first principles simulation during the actual process being performed. Meanwhile, the claimed processes and systems (by producing a first principles simulation result in a time frame shorter in time than the actual process being performed) permits accurate control of the process even if the system being controlled deviates from its historical behavior.

For all these reasons, Appellant submits that Claims 1, 8, and 75 patentably define over Sonderman et al and Jain et al and Tan et al.

Hence, the 35 U.S.C. § 103(a) rejection of Claims 1, 8, and 75 as being unpatentable over Sonderman et al in view of Jain et al and further in view of Tan et al should be reversed.

C. Regarding the 35 USC 103 Rejection of Claims 1-14, 20-21, 29-30, 32-34, 37-51, 57-58, 66-67, 69-71, 74-78, and 81 over Sonderman et al and Jain et al

Regarding the rejections over Sonderman et al and Jain et al, Appellant points out that the previous arguments given above as to the deficiencies of Sonderman et al and Jain et al and Tan et al likewise apply to the claims rejected under Sonderman et al and Jain et al.

Hence, the 35 U.S.C. § 103(a) rejection of 1-14, 20-21, 29-30, 32-34, 37-51, 57-58, 66-67, 69-71, 74-78, and 81as being unpatentable over Sonderman et al in view of Jain et al should be reversed.

D. Regarding the 35 USC 103 Rejection of Claims 15-19 and 52-56 over Sonderman et al and Jain et al

Furthermore, with regard to Claims 15-19 and 52-56 rejected as being obvious over Sonderman et al and Jain et al, Appellant specifically points out below the following deficiencies in Sonderman et al and Jain et al. Claims 15-19 are reproduced below for the sake of convenience:

> 15. The method of Claim 1, further comprising using a network of interconnected resources inside a semiconductor device manufacturing facility to perform the first principles simulation recited in Claim 1.
>
> 16. The method of Claim 15, further comprising using code parallelization among interconnected computational resources to share the computational load of the first principles simulation.
>
> 17. The method of Claim 15, further comprising sharing simulation information among interconnected resources to control the process performed by the semiconductor processing tool.
>
> 18. The method of Claim 17, wherein said sharing simulation information comprises distributing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principles simulations by different resources.
>
> 19. The method of Claim 17, wherein said sharing simulation information comprises distributing model changes among the interconnected resources to reduce redundant refinements of first principles simulations by different resources.

Claim 15 defines that a network of interconnected resources inside a semiconductor device manufacturing facility is used to perform the first principles simulation recited in Claim 1. The final Office Action on pages 18-19 cites to Sonderman et al (col. 5-8, col. 9, lines 60-65, and Col. 9, lines 58 onward) and cites to Jain et al (section III) for a disclosure of

these features.

Appellant points out that, while Sonderman et al shows a network in a semiconductor device manufacturing facility, this network includes as shown in Figure 1 of Sonderman et al only one computer system 130 for the receiving of data and updating of the manufacturing model. Hence, a network of interconnected resources inside a semiconductor device manufacturing facility is **not** used to perform a simulation result in Sonderman et al. Rather, only one computer resource (i.e., computer system 130) is used to calculate a simulation result.

Jain et al in section II describe a virtual mathematical physical engine (MPE) or dedicated MPE "consisting of hundreds or thousands of processors. Jain et al in section III describe a parallel architecture used in the MPE described therein. Section IV of Jain et al more specifically describes a networking of computational resources across the country, which it describes as "essential in the implementation of the virtual MPE."

Accordingly, Jain et al in teaching the essential use of networking across the country (probably for the reason of having access to hundreds or thousands of processors) ***teach away*** from Claim 15, where there is a network of interconnected resources i***nside a semiconductor device manufacturing facility*** that is used to perform the first principles simulation.

Hence, for this additional reason (besides their dependence from allowable claims), the 35 U.S.C. § 103(a) rejection of Claims 15-19 and 52-56 as being unpatentable over Sonderman et al in view of Jain et al should be reversed.

E. Regarding the 35 USC 103 Rejection of Claims 79 and 80 over Sonderman et al and Jain et al

Claim 79 defines that the performing a first principles simulation includes providing for the first principles simulation a reuse of known solutions as initial conditions for the first

principles simulation. The Office Action notes that "Jain teaches use of Navier Stokes and other known simulation solutions" and cites pp. 367-368 of Jain et al. However, the Navier Stokes equation on page 367 of Jain et al is a fluid flow equation which needs boundary conditions and which need s to be solved in order to produce a solution. The Navier Stokes equation on page 367 of Jain et al does **not** represent a solution, much less the reuse of known solutions as initial conditions for the first principles simulation. Appellant's inspection of the remainder of Jain et al finds no disclosure of the reuse of known solutions as initial conditions for the first principles simulation.

Hence, for this additional reason (besides their dependence from allowable claims), the 35 U.S.C. § 103(a) rejection of Claims 79 and 80 as being unpatentable over Sonderman et al in view of Jain et al should be reversed.

F. Regarding the 35 U.S.C. § 103 Rejection of Claims 22 and 59 over Sonderman et al, Jain et al, and Yunemura et al

The Office Action applies Yunemura et al to overcome the deficiencies of Sonderman et al and Jain et al regarding the features of Claims 22 and 59 directed to an ANSYS computer code. Yet, the claimed ANSYS computer code is utilized to perform the first principles simulation on the actual process being performed defined in Claim 1. Meanwhile, Yunemura et al describe first simulation modeling on a silicon chip. Thus, Yunemura et al is directed to heat generation and dissipation of heat from an operating silicon chip.

Thus, the ANSYS computer codes in Yunemura et al are not directed to modeling of a processing condition. Accordingly, one of ordinary skill in the art would have no rationale to consider or use Yunemura et al for process control.

Hence, for this additional reason (besides their dependence from allowable claims), the 35 U.S.C. § 103(a) rejection of Claims 22 and 59 as being unpatentable over Sonderman

et al, Jain et al, and Yunemura et al should be reversed.

G. Regarding the 35 U.S.C. § 103 Rejection of Claim 23-28 and 60-65 over Sonderman et al and Jain et al and Chen

The Office Action applies Chen to overcome the deficiencies of Sonderman et al and Jain et al regarding the features of Claims 23-28 and 60-65 of choosing a close fitting solution of the first principle simulation to thereby set initial conditions for cell in the first principle simulation. Yet, of the section cited in the Office Action from Chen (col. 5, line 38 to col. 6, line 25), Appellant points out that Chen's use of a fitting function described therein is for fitting simulated and measured data. There is no disclosure in Chen of:

> calculating a solution to the first principles simulation by applying a close-fitting solution to thereby set initial conditions for cells in the first principles simulation.

Specifically, there is no disclosure in Chen of 1) setting initial conditions in a first principles simulation, or 2) setting the initial conditions for cells in a first principles simulation. Thus, a combination of Chen with Sonderman et al and Jain et al would not yield these claim features.

Furthermore, there is no disclosure in Chen for the features defined in Claims 27-28 and 64-65 regarding choosing a coarse grid for a solution of the first principles simulation (Claims 27 and 64) and then using the solution for coarse grid in a fine grid simulation (Claims 28 and 65).

Thus, for all these reasons, a combination of Chen with Sonderman et al and Jain et al would not produce the feature in Claims 23-28 and 60-65.

Hence, for this additional reason (besides their dependence from allowable claims), the 35 U.S.C. § 103(a) rejection of Claims 23-28 and 60-65 as being unpatentable over Sonderman et al, Jain et al, and Chen should be reversed.

H. Regarding the 35 U.S.C. § 103 Rejection of Claims 31, 36, 68, and 73 over Sonderman et al and Jain et al and Nikoonahad

The Office Action applied Nikoonahad to overcome the deficiencies of Sonderman et al and Jain et al regarding the features of Claims 31, 36, 68, and 73. Yet, the examiner's position as to why it would have been obvious to combine Nikoonahad to Sonderman et al and Jain et al is merely a statement of the teachings being analogous art and both concerning modeling. Yet, KSR requires an articulated rationale as to why the claimed features are obvious and indicates that conclusory statements are not sufficient.

Thus, with no articulated reasons, the rejections of Claims 31, 36, 68, and 73 should be reversed.

I. Regarding the 35 U.S.C. § 103 Rejection of Claims 35 and 72 over Sonderman et al and Fatke

The Office Action applied Fatke et al to overcome the deficiencies of Sonderman et al regarding the features of Claims 35 and 72. Yet, the examiner's position as to why it would have been obvious to combine Fatke et al with Sonderman et al is merely a statement that the teachings are analogous art and the asserted existence in Fatke et al of one of the claimed elements, which the Office Action asserts can be applied to Sonderman et al.

Once again, the examiner uses only a conclusory statement. Thus, the rejection of Claims 35 and 72 should be reversed.

J. Regarding the Double Patenting Rejections

1. The Double Patenting Rejection over the '583 Application

The filed terminal disclaimer addressed this issue. Hence, Appellant has overcome the double patenting rejection.

2. The Double Patenting Rejection over the '501 Application

The filed terminal disclaimer addressed this issue. Hence, Appellant has overcome the double patenting rejection.

3. The Double Patenting Rejection over the '138 Application

The filed terminal disclaimer addressed this issue. Hence, Appellant has overcome the double patenting rejection.

VII. 41.37(c)(1)(vii) Claims Appendix Of Claims Involved In Appeal

Attached herewith is a Claims Appendix.

IX. 41.37(C)(1)(IX) Evidence Appendix

There is no evidence from the Appellant. Included in the appendix is a copy of Sushing Chen, "AEMPES: An expert system for in-situ diagnostics and process monitoring," referred to by the examiner, but not applied, in the Office Action of February 7, 2008.

X. 41.37(c)(1)(x) Related Proceedings Appendix

There are no related proceedings.

XI. Conclusion

Appellant request on the basis of the arguments presented above that the outstanding grounds for the rejection be reversed. Appellant submits that the application is in condition for allowance.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method of controlling a process performed by a semiconductor processing tool, comprising:

inputting process data relating to an actual process being performed by the semiconductor processing tool;

inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;

performing first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, said first principles simulation result being produced in a time frame shorter in time than the actual process being performed; and

using the first principles simulation result obtained during the performance of the actual process to control the actual process performed by the semiconductor processing tool.

2. The method of Claim 1, wherein said inputting process data comprises directly inputting the data relating to the actual process being performed by the semiconductor processing tool from at least one of a physical sensor and a metrology tool physically mounted on the semiconductor processing tool.

3. The method of Claim 1, wherein said inputting process data comprises indirectly inputting the data relating to the actual process being performed by the semiconductor processing tool from at least one of a manual input device and a database.

4. The method of Claim 3, wherein said indirectly inputting comprises inputting data recorded from a process previously performed by the semiconductor processing tool.

5. The method of Claim 3, wherein said indirectly inputting comprises inputting data set by a simulation operator.

6. The method of Claim 1, wherein said inputting process data comprises inputting data relating to at least one of the physical characteristics of the semiconductor processing tool and the semiconductor tool environment.

7. The method of Claim 1, wherein said inputting process data comprises inputting data relating to at least one of a characteristic and a result of a process performed by the semiconductor processing tool.

8. The method of Claim 1, wherein said inputting a first principles physical model comprises inputting a spatially resolved model of the geometry of the semiconductor processing tool.

9. The method of Claim 1, wherein said inputting a first principles physical model comprises inputting fundamental equations necessary to perform first principles simulation for a desired simulation result.

10. The method of Claim 1, wherein said performing first principles simulation comprises performing first principles simulation concurrently with the process performed by the semiconductor processing tool.

11. The method of Claim 1, wherein said performing first principles simulation comprises performing first principles simulation independent of the process performed by the semiconductor processing tool.

12. The method of Claim 1, wherein said performing first principles simulation comprises using the input data to set a boundary condition of the first principles simulation model.

13. The method of Claim 1, wherein said performing first principles simulation comprises using the input data to set an initial condition of the first principles simulation model.

14. The method of Claim 1, wherein said using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor processing tool.

15. The method of Claim 1, further comprising using a network of interconnected resources inside a semiconductor device manufacturing facility to perform the first principles simulation recited in Claim 1.

16. The method of Claim 15, further comprising using code parallelization among interconnected computational resources to share the computational load of the first principles simulation.

17. The method of Claim 15, further comprising sharing simulation information among interconnected resources to control the process performed by the semiconductor processing tool.

18. The method of Claim 17, wherein said sharing simulation information comprises distributing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principles simulations by different resources.

19. The method of Claim 17, wherein said sharing simulation information comprises distributing model changes among the interconnected resources to reduce redundant refinements of first principles simulations by different resources.

20. The method of Claim 1, further comprising using remote resources via a wide area network to control the semiconductor process performed by the semiconductor processing tool.

21. The method of Claim 20, wherein said using remote resources comprises using at least one of remote computational and storage resources via a wide area network to facilitate the semiconductor process performed by the semiconductor processing tool.

22. The method of Claim 1, wherein said performing first principles simulation utilizes at least one of an ANSYS computer code, a FLUENT computer code, a CFRDC-ACE computer code, and a direct simulation Monte Carlo computer code.

23. The method of Claim 1, wherein said performing first principles simulation comprises:

calculating a solution to the first principles simulation by applying a close-fitting solution to thereby set initial conditions for cells in the first principles simulation.

24. The method of Claim 23, wherein said calculating comprises:

selecting said close-fitting solution from a library of solutions.

25. The method of Claim 24, wherein said selecting comprises:

selecting a solution from the library of solutions that has proven convergence on the semiconductor processing tool.

26. The method of Claim 23, wherein said selecting comprises:

selecting said close-fitting solution from a library of solutions existing on a network of computers connected to said semiconductor processing tool.

27. The method of Claim 1, wherein said performing first principles simulation comprises:

calculating a solution to the first principles simulation by choosing a coarse grid for solution to the first principles simulation.

28. The method of Claim 27, wherein said calculating a solution further comprises:

utilizing the solution of the coarse grid to set initial conditions for cells in a subsequent first principles simulation using a fine grid.

29. The method of Claim 1, wherein said using the first principles simulation result to control the process comprises:

performing a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components.

30. The method of Claim 1, wherein said using the first principles simulation result to control comprises:

controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system , a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

31. The method of Claim 30, wherein said using the first principles simulation result to control comprises:

controlling at least one of a chemical vapor deposition system and a physical vapor deposition system.

32. The method of Claim 1, further comprising:

inputting as tool data at least one of etch rate, deposition rate, etch selectivity, an etch critical dimension, an etch feature anisotropy , a film property, a plasma density, an ion energy, a concentration of a chemical specie, a photoresist mask film thickness, a photoresist pattern dimension.

33. The method of Claim 1, wherein said inputting data comprises:

inputting physical geometric parameters of at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

34. The method of Claim 1, wherein said using the first principles simulation result to control comprises:

controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool.

35. The method of Claim 34, wherein said controlling comprises:

utilizing at least one of nonlinear optimization and multivariate analysis to derive a control model for process control.

36. The method of Claim 1, further comprising:

exchanging information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles simulation, and solution convergence history for said model solutions.

37. The method of Claim 1, further comprising:

inspecting process results; and

providing input to the first principles simulation for calibration purposes.

38. A system comprising:

a semiconductor processing tool configured to perform a process;

an input device configured to input data relating to an actual process being performed by the semiconductor processing tool; and

a first principles simulation processor configured to:

input a first principles physical model including a set of computer-encoded differential equations describing at least one of a basic physical or chemical attribute of the semiconductor processing tool, and

perform first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles

simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, said first principles simulation result being produced in a time frame shorter in time than the actual process being performed, wherein said first principles simulation result obtained during the performance of the actual process is used to control the actual process performed by the semiconductor processing tool.

39. The system of Claim 38, wherein said input device comprises at least one of a physical sensor and a metrology tool physically mounted on the semiconductor processing tool.

40. The system of Claim 38, wherein said input device comprises at least one of a manual input device and a database.

41. The system of Claim 40, wherein said input device is configured to input data recorded from a process previously performed by the semiconductor processing tool.

42. The system of Claim 40, wherein said input device is configured to input data set by a simulation operator.

43. The system of Claim 38, wherein said input device is configured to input data relating to at least one of the physical characteristics of the semiconductor processing tool and the semiconductor tool environment.

44. The system of Claim 38, wherein said input device is configured to input data relating to at least one of a characteristic and a result of a process performed by the semiconductor processing tool.

45. The system of Claim 38, wherein said processor is configured to input a first principles physical model comprising a spatially resolved model of the geometry of the semiconductor processing tool.

46. The system of Claim 38, wherein said processor is configured to input a first principles physical model comprising fundamental equations necessary to perform first principles simulation for a desired simulation result.

47. The system of Claim 38, wherein said processor is configured to perform said first principles simulation concurrently with the process performed by the semiconductor processing tool.

48. The system of Claim 38, wherein said processor is configured to perform said first principles simulation not concurrently with the process performed by the semiconductor processing tool.

49. The system of Claim 38, wherein said processor is configured to perform said first principles simulation at least by using the input data to set a boundary condition of the first principles simulation model.

50. The system of Claim 38, wherein said processor is configured to perform said first principles simulation at least by using the input data to set an initial condition of the first principles simulation model.

51. The system of Claim 38, wherein said processor is configured to use the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor processing tool.

52. The system of Claim 38, further comprising a network of interconnected resources inside a semiconductor device manufacturing facility and connected to said processor and configured to assist said processor in performing at least one of the inputting a first principles simulation model and performing a first principles simulation.

53. The system of Claim 52, wherein said network of interconnected resources is configured to use code parallelization with said processor to share the computational load of the first principles simulation.

54. The system of Claim 52, wherein said network of interconnected resources is configured to share simulation information with said processor to facilitate said process performed by the semiconductor processing tool.

55. The system of Claim 54, wherein said network of interconnected resources is configured to distribute simulation results to said processor to reduce redundant execution of substantially similar first principles simulations.

56. The system of Claim 54, wherein said network of interconnected resources is configured to distribute model changes to said processor to reduce redundant refinements of first principles simulations.

57. The system of Claim 38, further comprising remote resources connected to said processor via a wide area network and configured to facilitate the semiconductor process performed by the semiconductor processing tool.

58. The system of Claim 57, wherein said remote resources comprise at least one of a computational and a storage resource.

59. The system of Claim 38, wherein said processor is configured to perform first principles simulation utilizes at least one of an ANSYS computer code, a FLUENT computer code, a CFRDC-ACE computer code, and a direct simulation Monte Carlo computer code.

60. The system of Claim 38, wherein said processor is configured to perform first principles simulation at least by calculating a solution to the first principles simulation by applying a close-fitting solution to thereby set initial conditions for cells in the first principles simulation.

61. The system of Claim 60, wherein said processor is configured to perform said calculating by at least selecting said close-fitting solution from a library of solutions.

62. The system of Claim 61, wherein said processor is configured to perform said selecting by at least selecting a solution from the library of solutions that has proven convergence on the semiconductor processing tool.

63. The system of Claim 60, wherein said processor is configured to perform said selecting by at least selecting said close-fitting solution from a library of solutions existing on a network of computers connected to said semiconductor processing tool.

64. The system of Claim 38, wherein said processor is configured to perform first principles simulation by at least calculating a solution to the first principles simulation by choosing a coarse grid for solution to the first principles simulation.

65. The system of Claim 64, wherein said processor is configured to perform calculating a solution by at least utilizing the solution of the coarse grid to set initial conditions for cells in a subsequent first principles simulation using a fine grid.

66. The system of Claim 38, wherein said processor is configured to use the first principles simulation result to control the process by at least performing a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components.

67. The system of Claim 38, wherein said processor is configured to use the first principles simulation result to control the process by at least controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

68. The system of Claim 67, wherein said processor is configured to use the first principles simulation result to control the process by controlling at least one of a chemical vapor deposition system and a physical vapor deposition system.

69. The system of Claim 38 wherein said input device is configured to input at least one of etch rate, deposition rate, etch selectivity, an etch critical dimension, an etch feature anisotropy, a film property, a plasma density, an ion energy, a concentration of a chemical specie, a photoresist mask film thickness, a photoresist pattern dimension.

70. The system of Claim 38, wherein said input device is configured to input physical geometric parameters of at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

71. The system of Claim 38, wherein said processor is configured to use the first principles simulation result to control the process by at least controlling the semiconductor

processing tool by using model output to adjust said process performed by the semiconductor processing tool.

72. The system of Claim 71, wherein said processor configured to perform said controlling by utilizing at least one of nonlinear optimization and multivariate analysis to derive a control model for process control.

73. The system of Claim 38, wherein said processor is further configured to exchange information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles simulation, and solution convergence history for said model solutions.

74. The system of Claim 38, wherein said processor is further configured to:

inspect process results; and

provide input to the first principles simulation for calibration purposes.

78. At least one of non-volatile media and volatile media containing program instructions for execution on a processor, which when executed by the computer system, cause the processor to perform the steps of:

inputting process data relating to an actual process being performed by the semiconductor processing tool;

inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;

performing first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, said first principles simulation result being produced in a time frame shorter in time than the actual process being performed; and

using the first principles simulation result obtained during the performance of the actual process to control the actual process being performed by the semiconductor processing tool.

79. The method of Claim 1, wherein said performing a first principles simulation comprises:

providing for the first principles simulation a reuse of known solutions as initial conditions for the first principles simulation.

80. The system of Claim 38, wherein the first principles simulator is configured to provide for the first principles simulation a reuse of known solutions as initial conditions for the first principles simulation.

EVIDENCE APPENDIX

1. Su-shing Chen, "AEMPES: An expert system for in-situ diagnostics and process monitoring," See Office Action of February 7, 2008.

AEMPES: An expert system for in-situ diagnostics and process monitoring

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Abstract

An expert system - ***AEMPES*** (Advanced Electronic Materials Processing Expert System) for in-situ diagnostics and process monitoring, is being developed. This expert system is a key component of the ***intelligent manufacturing equipment architecture*** which is proposed to integrate the manufacturing line with its simulator. In the expert system, there are two interrelated subsystems - a ***neural network*** subsystem for adaptive process control, monitoring, and learning, and a ***rule-based*** subsystem for human interface and high-level AI reasoning.

1. Introduction

An intelligent manufacturing equipment architecture was defined in [2]. In [5], [10], an idea to implement this architecture was proposed. It has two components:

(1) manufacturing equipment - equipment hardware and sensors,
(2) intelligent expert workstation - a hybrid AI/neural network expert workstation.

For the intelligent expert workstation, we propose the philosophy of a hybrid AI/neural network expert workstation. Its model-based reasoning scheme contains process models and the equipment model. A neural network simulation software is used to learn process models and the equipment model (Sometimes, human expert knowledge is very useful to prescribe the network topology so that the learning is supervised). A neural network hardware emulates the process models and the equipment model for adaptive and on-line process monitoring and control. A rule-based expert system provides human interface and high-level decision support.

We have discovered that a manufacturing line can be integrated with its manufacturing line simulator at the intelligent expert workstation level. An intelligent expert workstation provides a link between the manufacturing line and its simulator at the equipment module. In essence, the manufacturing line is distributed into clusters of processing modules, each of which has an intelligent expert workstation described above. At present, manufacturing (hardware) lines and their (software) simulators are separately functioning [1].

The organization of this paper is as follows. In section 2, some important issues of manufacturing automation are discussed. In section 3, the distributed AEMPES system is described. We refer to [7] for a related result on group technology in semiconductor design for manufacturing. In section 4, the intelligent equipment architecture is proposed. In section 5, the ideas of implementing an individual AEMPES expert workstation are presented. In addition to the neural network methodology, qualitative simulation, discussed in [6], is also quite useful in the model-based reasoning. In section 6, a neural network software - INNSE (Interactive Neural Network Simulation Environment) is presented. INNSE is a subset of the expert workstation. More detailed modeling results of processes and equipment will appear elsewhere.

2. Manufacturing Automation

In manufacturing automation, two major objectives are the tight coupling of CAD/CAM/CAT and the integration of a manufacturing line and its simulator [1], [2]. First, in manufacturing automation, the design, manufacturing and testing should not be separate stages. There are at least two reasons:

(1) The flow of the complete fabrication process relies on the synchronization of many steps in the three stages.
(2) The tight coupling of three stages enables the control, scheduling, and management of the complete fabrication process to be more effective and adaptive.

The tight coupling requires simultaneous considerations of manufacturing process design and relevant device design, an enormous endeavor. At present, we do not know exactly how to couple the three stages tightly. However, the starting point should be the modeling of equipment and processes and the interface of equipment/process models with CAD and CAT data.

Secondly, the integration of a manufacturing line and its simulator is essential to autonomous manufacturing systems, because the manufacturing line simulator may be considered as the "brain" which maintains the central intelligence of a manufacturing system. The autonomous (human like) behavior of a manufacturing system is manifested by the level of integration of its "brain" and its "arms and legs".

The integration enables adaptive sensor-driven control, learning, planning, and optimization in production. At present, we do not have complete integration of manufacturing lines with their simulators. The main reason is the lack of a linking point between the two.

An equipment model is the computational model of a semiconductor fabrication equipment, such as an optical lithography stepper or an ion implanter. Because of the diversity of semiconductor fabrication equipment, their models should have an open architecture that is developable using rapid prototyping techniques. Moreover, these models should be multifunctional for assisting manufacturing engineers, process engineers and operators.

3. Distributed System - AEMPES

The logical architecture of AEMPES depends on the clustering of process modules and the interconnection of different clusters. A vacuum wafer transport system is being developed for interconnecting different clusters. Within each cluster, processing modules are completely integrated in the Brooks mechanism. Providing each processing module with an expert system, we require a central expert workstation composing of these individual expert systems. The characterization, testing and diagnostics measurement and process control are performed in the central expert workstation. Indeed, this is a tightly coupled cluster.

Nontheless, monitoring, control and diagnostics of the collection of all cluster subsystems are quite different. Physically, the local area network interconnecting those subsystems is in parallel with the vacuum wafer transport system. Due to the complexity of semiconductor processing, a centralized explicitly constrained and minimally adaptive approach may not be adequate. A distributed system consisting of interacting and coordinating cluster expert workstation is necessary. Thus, techniques in distributed AI systems are used in the global AEMPES.

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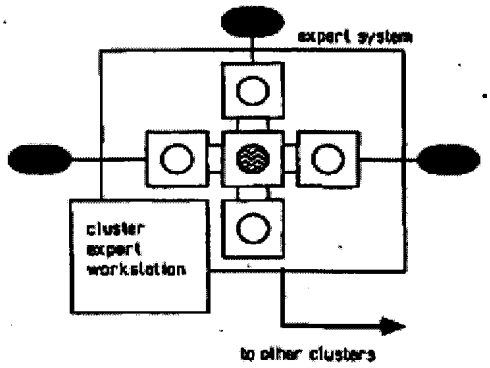


Distributed AI mechanisms are quite complex. Some of the issues include:

(1) Accomodation of open systems (systems with no complete representation and with dynamically changing boundaries).
(2) Combinatorial implosion, the possibility that partial results at one cluster in the system may greatly constrain the potential solution space at another cluster.
(3) Adaptability, the possibility that concurrent systems are inherently more adaptable than sequential systems.
(4) Multiple perspectives, the need to make different viewpoints consistent.
(5) Modeling and analysis of coordinating intelligent agents are different from usual methodologies.

Often global system information is needed by clusters to make local decisions because of interdependency of different clusters. There is no universal global optimization criterion. We propose the cooperative Pareto optimization scheme. Intuitively, it is a scheme which optimizes multiple objective functions of different clusters. A solution to the Pareto optimization problem is one which does not allow preferential treatment of any individual cluster. If a certain priority is used in the overall factory planning, this scheme must be modified. Otherwise, the sequencing of processing tasks follows this scheme.

Associated with this distributed AI approach, there are the issues of data communication network standard and databases. The SEMI Equipment Communications Standard (SECS) is extendible to this case. A distributed database fits naturally into the distributed AI setting. In fact, it is a subset of the distributed expert system.

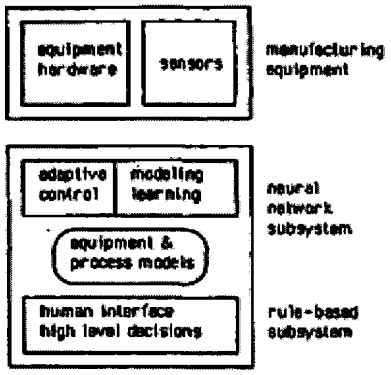
4. Intelligent Equipment Architecture

The intelligent equipment architecture consists of two components:

(1) manufacturing equipment - equipment hardware and sensors.
(2) intelligent expert workstation - a hybrid AI/neural network expert workstation.

For the intelligent expert workstation, we propose the philosophy of a hybrid AI/neural network expert workstation. Its model-based reasoning scheme contains process models and the equipment model. A neural network simulation software is used to learn process models and the equipment model. A neural network hardware emulates the process models and the equipment model for adaptive and on-line process monitoring and control. A rule-based expert system provides human interface and high-level decision support.

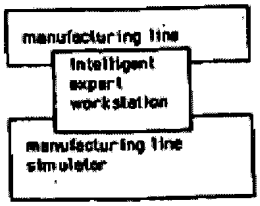
The neural network subsystem which emulates the process/equipment models serves as the "intelligent controller" of the equipment module. The intelligent controller has real-time links with VLSI integrated sensors and actuators of the fabrication equipment. Thus, the manufacturing line and its simulator are tightly integrated in a close-loop manner.



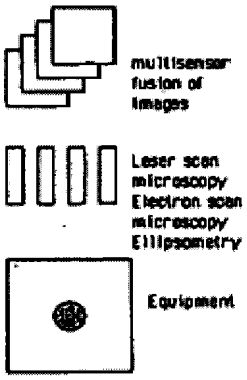
Intelligent equipment architecture

Close-loop feedback control at each equipment module requires in-process inspection, testing and characterization. Laser scan microscopy, electron scan microscopy, ellipsometry, and interferrometry could provide in-process data for extraction of spatial information, such as linewidths and thickness, and to inspect particulate-induced defects. The expert workstation has to determine whether a given equipment parameter is within certain specifications from the extracted feature values. We could investigate multisensor fusion so that more complete spatial information is obtained. Furthermore, electrical C-V measurements are fused with sensed image data, and their spatial interpretations.

The learning and optimization capabilities are supported by the neural network subsystem of the intelligent expert workstation. However, a neural network system alone cannot provide complete solutions to complex engineering problems. A hybrid AI/neural network expert system is proposed here to capture manufacturing knowledge, to perform adaptive control, and to make planning and decision support, interacting with the manufacturing simulator.



Integration of manufacturing line and its simulator



5. AEMPES: Real-time Diagnostics and Control

In each cluster, AEMPES is to capture the capability of experienced process engineers for diagnostics, monitoring, and control of the cluster of equipment modules. This experience is integrated with computer analysis capability and basic models of the underlying physics of the cluster of equipment modules. The knowledge required is coded into AEMPES for assisting process operators or autonomously monitor/control the fabrication processes.

In AEMPES, we use the concept of model-based reasoning. Model-based reasoning is an extension of rule-based expert system technology [3]. It is a subfield of knowledge engineering that involves building and analyzing an explicit computational model of the structure, principles and behavior of a system. In a traditional rule-based expert system, heuristics used by an expert to solve a particular problem are coded into the knowledge base. In a model-based system, knowledge is represented explicitly in computational models. Model-based reasoning is more flexible, because the same system model may be used for different applications of a cluster expert workstation:

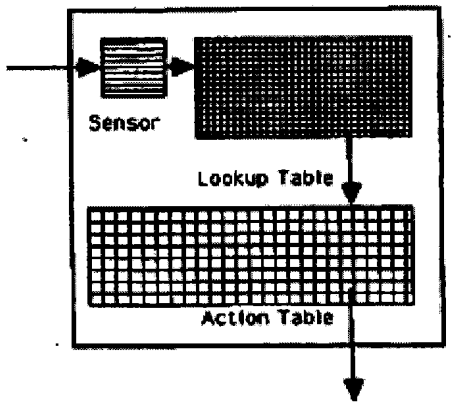
Diagnostics,
Sensor/actuator interface,
CAD/CAT interface,
Human operator interface,
Planning,
Decision support,
Control,
Analysis.

It is possible to integrate different perspectives of various applications in a single model. This increases the power of an expert system. Furthermore, model-based reasoning systems may be extended and modified quite easily to reflect any change in the processing and overall manufacturing environment. Traditional rule-based reasoning systems can only be changed by rewriting a significant amount of codes. Model-based systems are algorithm-based. Algorithms can be revised continuously in computational models by human expert or machine learning (using both AI and neural network approaches).

Conventional model-based reasoning systems are object-oriented [3]. Structural elements of a model may include:

Concepts (modules and submodules)
Objects (sensors, components in a submodule)
Attributes (parameters -temperature, voltage, pressure)
Relations (A is a component of B, B is a subsystem of C)
Functions (thermal oxidation, cleaning)

For example, in the application of diagnostics, functions are represented from the perspective of component faults on the functions. The values of a component attribute determine whether a component is normal or not. Simple programs can be embedded in each breakable component to create a "test-case generator" that automates fault analysis and simulation.



The object oriented trees of model-based reasoning can be represented by neural networks. Conversely, knowledge in neural networks can be represented by semantic networks in object-oriented forms. This has been established in the literature. See also [8,9] and [11,12]. However, in some neural network modeling techniques (e.g. the back propagation technique), additional internal variables are introduced and models involving additional variables are learned. Although these variables may not have immediate physical interpretations, we consider them as essential process/equipment parameters. See the next section for some modeling examples.

6. Interactive Neural Network Simulation Environment

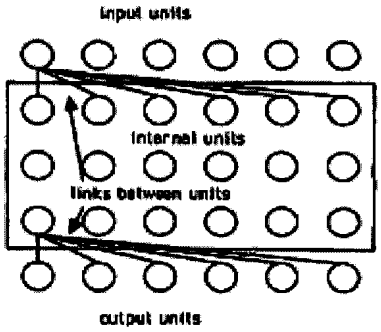
Interactive Neural Network Simulation Environment (INNSE) is a hierarchical neural network simulator, with its macrocells constructed by users, is capable of modeling equipment, processes, and manufacturing lines, and is capable of simulation run as flow of activation networks. As CAD tools for circuit design engineers, INNSE is a part of the manufacturing process design software environment in the intelligent expert workstation described above.

Each neural network model consists of a set of input units and output units, a set of internal units, a transition rule, and a learning rule. There may be as many layers of internal units as we wish.

Let us denote by (v_i) the input units, (v_j) the output units, and (v_k) the internal units. The values to be assumed are between 0 and 1. This requires a scaling factor for each physical variable. The link weights between these units are denoted by λ_{ik} and λ_{kj}, indicating connections between input units, internal units, and output units. The link weights assume values between -1 and +1. A positive link weight indicates exitatory connection, and a negative link weight indicates inhibitory connection.

For illustration, we discuss two examples. The first is a neural network model of the thermal oxidation process. In [13], a power law was proposed for the oxidation thickness:

$$x = at^b,$$



where a and b are functions of the temperature T and the pressure p, and t is the time. A more detailed power law involves with the initial thickness x_0 and the initial time t_0. It was shown that the power law fits all observed data in thermal oxidation [13]. Easily, we have modeled the functions a and b as output units of a neural network with input units T, p, x_0, t_0. Using a back propagation learning rule, we can construct this network with 10 internal units within error rate of 1%. This network can predict the behaviors of a and b under input values which have not been experimented. The thickness x can also be determined for unexperimented input values, by either the power law or a neural network of itself (x is treated as a function of T, p, x_0, t_0). In future work, we shall verify our results with experimental data. If successful, we shall use this network for multiple-stage oxidation analysis and control.

The second example is the neural network modeling of the Balzers SWS 605 system. It is a single wafer, cassette-to-cassette, planar magnetron sputtering system. This model is a first phase modeling result. In the later phases, we plan to incorporate expert knowledge into the modeling process, resulting in more sophisticated neural network models. In the present phase, we consider 2 input units - power and gas pressure, and 5 output units - Aluminum deposition rate, TiW deposition rate, metal film stress, sputter etch uniformity, and sputter etch rate. Of 12 internal units, we have constructed the neural network within error rate of 1 %. This rather simple model provides a basic function of this equipment.

7. Conclusion

In this paper, we have presented a framework of the intelligent equipment architecture and a neural network modeling methodology. Neural network representations can be translated into the conventional AI reasoning mechanisms for developing the intelligent expert workstation - AEMPES. The present statistical modeling techniques, such as regression analysis and factorial design, do not have this capability. The more important issue is the real-time, close-loop control in the intelligent equipment architecture. We have proposed the same neural networks to serve as the controller [9].

We would like to express our gratitude to SRC and NSF-ERC for their partial financial support. We are also indebted to Jon Fitch of NCSU for his papers and unpublished data on the Balzers system.

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RELATED PROCEEDINGS APPENDIX

None